In the Specification

Please amend the applicants' specification as indicated below:

Page 2, 1st Paragraph

This application is a continuation-in-part of U.S. Patent Application Serial No. 09/654,643, now U.S. Patent Number 6,772,351, entitled "Low Latency Equalization in Multi-Level, Multi-Line Communication Systems," filed September 5, 2000, and, further, of U.S. Patent Application Serial No. 09/655,010, entitled "Method and Apparatus for Calibrating a Multi-Level Current Mode Driver," filed on September 5, 2000, which claims priority to U.S. Provisional Patent Application Serial No. 60/158,189, entitled "A Method and Apparatus for Receiving High Speed Signals with Low Latency," filed on October 19, 1999, the contents of each of which are incorporated herein by reference. Further, this application claims priority to a PCT Application No. ~~XXXX/XXXXX,~~ PCT/US01/27478, entitled "Method and Apparatus for Calibrating a Multi-Level Current Mode Driver and for Generating a Multi-Level Reference Voltage in Systems Using Equalization or Crosstalk Cancellation," filed on September 5, 2001, the contents of which are incorporated herein by reference. Additionally, the application incorporates in its entirety, U.S. Patent Application Serial No. 09/478,916, entitled "Low Latency Multi-Level Communication Interface," which claims priority to the U.S. Provisional Patent Application Serial No. 60/158,189, entitled "A Method and Apparatus for Receiving High Speed Signals with Low Latency."

Page 3, 3rd Paragraph

While many prior buses were driven by voltage level signals, it has become advantageous to provide buses that are driven by a current mode output driver. A benefit associated with a current mode driver is a reduction of peak switching current. In particular, the current mode driver draws a known current regardless of load and operating conditions. A further benefit is that the current mode driver typically ~~supresses~~ suppresses noise coupled ~~form~~ from power and ground supplies.

Page 15, 1st Paragraph

Hereinafter, systems and method for ~~generation~~ generating reference voltages will be described in reference to multi-PAM systems. However, it should be understood that the methods and systems are equally applicable in 2-PAM systems.

Page 20, 1st Complete Paragraph

Figure 7 illustrates the addition of a different equalization signal 3S, 2S, or S to the main signal when driving different transitions to compensate for the attenuation of the received signal. The equalization ~~signal~~ signals in this embodiment are transitory, so that each signal may, for example, have a duration less than or equal to one bit signal, after which the equalization signal is terminated, allowing the initially overdriven signal to maintain a steady state logic level. In other words, the equalization signals S, 2S or 3S add predetermined high-frequency components to the transition signals that raise the slope of the edge of transition. However, a difficulty with this approach for a system such as shown in Figure 3 is that the voltage can only be pulled down from the V_{TERM}, unless negative current could flow through the current sources 421, 422, and 423. In other words, with the 00 level set at the V_{TERM}, as illustrated in Figure 2, it is difficult for the equalization signals S, 2S or 3S to add to the transition above the V_{TERM}.

Page 21, Last Paragraph

In order to transition from the initial state 00 (0M+3S) to the final state 10 (3M+3S), for example, an overdriven transition drive signal of 3M+3S is provided. Conversely, changing from the initial state 10 (3M+0S) to the final state 00 involves a drive signal of 0M+0S. Table 1 illustrates one set of transition drive signals specific to a 4-PAM signaling system with a single error correction. However, it should be understood that the illustrated set of transition signals may be extrapolated to be used with communication systems having additional signal levels and additional error corrections. Further, it should be understand that similar transition drive signals could also be used in 2-PAM systems with ~~equalizaiton~~ equalization.

Page 22, 1st Paragraph

Figure 9 is a schematic block diagram illustrating an exemplary device 700 that may provide

the transition drive signals shown in Figure 8. An encoder 702 receives binary MSB and binary LSB signals and converts pairs of those 2-PAM signals into digital input signals along lines C1, C2 and C3 for a main driver 705 having three current sources ~~705~~ 711, 712, and 713, to convert the binary data of the MSB and LSB into 4-PAM data at an output pad 715. As illustrated in Figure 9, a delay mechanism 718 also receives the input signals from the encoder 702. The delay mechanism 718 inverts and delays the input signals by a one-bit signal period to feed signals E1, E2, and E3 to an auxiliary driver 720 including auxiliary driver current sources 721, 722, and 723 that are similar to the respective main driver current sources 711, 712 and 713. However, each auxiliary driver current source 721, 722, and 723 has a gain that is a fraction of the respective main driver current sources 711, 712, and 713. Thus, when the main driver 705 outputs an output signal, the auxiliary driver 720 outputs a signal that is delayed, inverted and proportional to the output signal of the driver 705. The signals generated by ~~the driver~~ drivers 705 and 720 combine at the line 728 to form a desired signal. A detailed description of a preferred equalization system can be found in the co-pending U.S. Patent Application Serial No. 09/654,643, entitled "Low Latency Equalization in Multi-Level, Multi-Line Communication Systems," identified above. The preferred embodiments, however, are applicable to systems using other types of equalization, and the invention should not be construed as limited to systems including the described equalization methods.

Page 22, the last paragraph bridging pages 22 and 23

Referring to Table 1, the main driver 705 can be represented with the letter M and the auxiliary driver 720 can be represented with the letter S, with the numeral proceeding each letter describing how many of the respective current sources are active. A ratio of the gain of the auxiliary driver, S, to that of the main driver, M, is termed k, the equalization coefficient of the auxiliary driver. The ratio k is less than one, and may range from about one percent to about fifty percent. Thus, the driving device on the bus ~~know~~ knows the equalization current based on the equalization coefficient set on the auxiliary driver. In one embodiment, the drivers 705 and 720 and the delay element 718 of Figure 9 may be represented as an FIR filter, where the input signals from the encoder 702 are sent to the filter, which operates on the signals to output a filtered signal.

Page 23, 1st complete paragraph

Equalization techniques similar to those described above for the attenuation can be used to compensate for crosstalk and reflection errors. Figure 10 and Figure 11 including Figures 11A, 11B, 11C, 11D and 11E, show a general system using a self equalization FIR filter 806 and crosstalk (XTK) equalization FIR 804 and crosstalk equalization FIR filter 802 for filtering errors on a line V(n) due to crosstalk from adjacent lines $A_1(n)$ through $A_J(n)$, respectively, to produce equalized output ~~V_{OUT} (N).~~ V(N).

Page 24, 1st complete paragraph

Figure 12 illustrates an exemplary electrical schematic of a device 900 that may be coupled to a device illustrated in Figure 9 and can be used to equalize inductive or capacitive errors created by signals in line 728 and sensed in lines that are adjacent to the line 728. A first crosstalk equalization driver 905 receives signals along lines ~~P1, P2 and P3~~ C1,C2 and C3 that have been inverted by inverters 910 controlling current sources 711, 712, and 713. The combined current from the current sources 911, 912, and 913 is output on a crosstalk equalization line 920 that is connected to an adjacent line, not shown, that is subjected to crosstalk errors from the line 728. The output on the line 920 from the driver 905 is thus scaled and inverted compared to the signal produced by the main driver 705, much like the signal 906 of Figure 11D is [[~~a~~]] scaled and inverted compared to the signal 900 in Figure 11A.

Page 26, 2nd complete paragraph

Figure 13 illustrates a 4-PAM voltage generator 1000 that generates the multi-PAM reference voltages V_{REFHI}, V_{REFM} and V_{REFLO} on respective reference-voltage nodes 1008, 1010, and 1012 from the external voltage V_{TERM} supplied on a voltage pin 1002 using a voltage divider, where the reference voltage levels reflect the shifts in the logic state level shifts in a system employing equalization and/or crosstalk signals. The voltage divider, including series-connected resistors R1, R2, R3, and R4, is coupled between the voltage pin 1002 supplying the V_{TERM} and a voltage pin 1006 supplying a V_{GROUND}.

Page 29, the last paragraph bridging pages 29 and 30

Similarly, to generate the V_{REFM} voltage level, a current driver 1158 drives into a terminating resistor R_{TERM} ~~1114~~ 1116 three-fourths of the current that would normally be driven to generate the logical state 11 under the Gray code system, and, further, shifts the V_{REFM} level according to the equalization and crosstalk current applied on the chip. Thus, the current driver 1140 drives a current I/2 to generate the V_{REFM} level that is further shifted by the current driver 1142 to compensate for the equalization and crosstalk. Finally, as illustrated in Figure 15, to generate the V_{REFLO} voltage level, a current driver 1160 drives into a terminating resistor R_{TERM} 1114 five-sixth of the current that would normally be driven to generate the logical state 10 under the Gray code system and, further, shifts the V_{REFLO} level according to the equalization and crosstalk currents applied on the chip. Thus, the current driver 1140 drives a current $5/6 \cdot I$ to generate the V_{REFLO} level that is further shifted by the current driver 1146 to compensate for the equalization and crosstalk. According to one embodiment, the equalization currents 1136, 1142 and 1146 are equal to the voltage shift used to compensate for crosstalk and equalization.